REMARKS

Claims 1-4, 7-10, 13-17 and 20-21 are currently pending.

Claims 1-4, 7-10, 13-17 and 20-21 have been rejected.

Claims 22-42 have been previously withdrawn.

Claim 1 has been amended.

Reconsideration of Claims 1-4, 7-10, 13-17 and 20-21 is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1, 2, 4, 7, 8, 10, 13-17 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,108,945 to James A. Matthews (hereinafter "*Matthews*"). In response, the Applicants have amended Claim 1.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

The limitations in amended Claim 1 are not taught or suggested in the *Matthews* reference. In particular, Matthews does not teach or suggest that a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain

substantially identical dopant concentrations in a semiconductor apparatus comprising a first polysilicon layer and a second silicon layer that is separate from the first polysilicon layer, as required by amended Claim 1.

For reference purposes, the Applicants set forth below an outline of certain major steps in the manufacture of the Applicants' invention.

A. Paragraph [00112] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the PNP device and an NMOS gate in the NMOS device.

B. Paragraph [00114] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the NPN device and a PMOS gate in the PMOS device.

C. Paragraph [00129] describes how the intrinsic base (3410) in the NPN device is doped and how the lightly doped drains (LDD) (3420, 3430) in the PMOS device are doped.

D. Paragraph [00132] describes how the intrinsic base (3510) in the PNP device is doped and how the lightly doped drains (LDD) (3520, 3530) in the NMOS device are doped.

E. Paragraph [00138] describes how the Poly 2 layer (3800) is doped to form (1) NPN emitter 3910 in the NPN device, and (2) NPN deep collector 3920 in the NPN device, and (3) NMOS source/drain 3930 in the NMOS device, and (4) PMOS well contact 3940 in the PMOS device.

F. Paragraph [00141] describes how the Poly 2 layer (3800) is doped to form (1) PNP emitter 4010 in the PNP device, and (2) PNP deep collector 4020 in the PNP device, and (3) NMOS well contact 4030 in the NMOS device, and (4) PMOS source/drain 4040 in the PMOS device.

The *Matthews* reference describes a device in which the first and second polysilicon layers are not separate. The first protective polysilicon layer 26 is deposited on field oxide layer 28. Then a second layer of polysilicon 31 is deposited over the first polysilicon layer 26 (*Matthews*, Column 10, Lines 6-8). The two layers fuse together. This is indicated by the fact that although the layer 31 is shown as planar in Figures 7A and 7B, there is actually a step in the surface due to the underlying layer 26. "The height of the step being equal to the thickness of the protective poly layer 26 (see FIGS. 6A and 6B) plus the thickness of the gate oxide." (*Matthews*, Column 10, Lines 34-37).

Then spaces 38 are etched out of the polysilicon layer 31. After the spaces 38 have been etched out an amorphous polysilicon is used to fill in the spaces. (*Matthews*, Column 11, Lines 28-32). The polysilicon that fills the spaces becomes part of the polysilicon layer 31. Therefore, the *Matthews* reference does not disclose a separate first polysilicon layer and a separate second silicon layer. The *Matthews* reference discloses that a third polysilicon layer is used to form polysilicon resistors that are adjunct to but not part of the transistor circuits. (*Matthews*, Abstract).

For the reasons set forth above, the Applicants respectfully submit that the *Matthews* reference does not teach or suggest the claimed elements of the Applicants' invention.

Accordingly, the Applicants respectfully traverse all of the anticipation rejections of Claims 1, 2, 4, 7, 8, 10, 13-17 and 20 and respectfully requests the Examiner to withdraw the § 102 rejections.

Claims 1-3, 7, 9, 13 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,091,760 to Maeda et al. (hereinafter "*Maeda*"). In response, the Applicants have amended Claim 1.

The *Maeda* reference describes a device in which the first and second polysilicon layers are not separate. A first polysilicon layer 24 is deposited on a gate oxide film 23 of the *Maeda* device. (*Maeda*, Column 4, Lines 26-29). Then a second layer of polysilicon 55 is deposited over the first polysilicon layer 24 (*Maeda*, Column 4, Lines 37-40). The two layers fuse together. This is indicated by the statement "First polysilicon layer 24 has been omitted from FIGS. 1F-1H in order to simplify the drawings." (*Maeda*, Column 4, Lines 42-44). Therefore, the *Maeda* reference does not disclose a separate first polysilicon layer and a separate second silicon layer.

For the reasons set forth above, the Applicants respectfully submit that the *Matthews* reference does not teach or suggest the claimed elements of the Applicants' invention. Reconsideration and allowance of the pending claims (Claims 1-4, 7-10, 13-17 and 20-21) are respectfully requested.

DOCKET NO. P05792 (NATI15-05792)
SERIAL NO. 10/777,012
PATENT

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckcarter.com*.

No fees are believed to be necessary. However, in the event that any fees are required for the prosecution of this application (including extension of time fees), the Commissioner is hereby authorized to charge any necessary fees to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

Date: June 2, 2008

William A. Munck
Registration No. 39,308

Docket Clerk
P.O. Drawer 800889
Dallas, Texas 75380
Tel: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@munckcarter.com*